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| EXAMINER |
|---|
| CRAIG, DWIN M |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/469,754 | Applicant(s) TSUKAMOTO ET AL. |
|---|---|---|
| | Examiner Dwin M Craig | Art Unit 2123 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *14 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

**1.** Claims 1-39 have been presented for reconsideration in light of Applicant's amended specification. After reconsideration Claims 1-33 are rejected.

### ***Response to Arguments***

**2.** Applicant's arguments filed on 14 March 2003 have been fully considered. Examiners response is a s follow:

**2.1** Regarding applicants response to Examiners request for clarification concerning the addition of new matter in respect to Application No. 08/879,696 which the Applicant is claiming benefit of priority to.

The Applicant has argued that;

> The Office Action notes that the application is a continuation-in-part of Application No. 08/879,696 which has issued as U.S. Patent No. 6,094,527 to Tsukamoto et al. The Office Action states that there does not appear to be new matter in the subject application as compared with the disclosure in U.S. Patent No. 6,094,527. The Office Action further states that the addition of reader/writer 16 and removable storage media 16a in Fig. 2 do not constitute the addition of new matter because hard disk 13 contains computer readable media with read/write ability.
>
> In view of the remarks in the Office Action, it is Applicants' understanding that the Examiner deems the claims of the subject application to be fully supported by, and therefore is entitled to the benefit of priority of, parent application no. 08/879,696.
>
> Applicants respectfully direct the Examiner's attention to, for example, the specification at page 6, line 7 through page 7, line 7 which further describe elements 16a and 16.

The Examiner asserts that by *applicants own admission* there is no new matter being presented in the application currently under consideration. The Examiner asserts that the only new matter being disclosed by application 09/469754 is the use of a DVD or (Digital Video Disk) as disclosed on *page 4 line 21* of Applicant's application this is because the use of DVD as a storage medium did not begin until 1997. The Examiner asserts that the use of CDROM as a

computer storage media and the use of floppy disks where known in the art before the filing of application 09/469754 and are therefore NOT considered new matter by the Examiner because, *storage media* was disclosed in the Applicant's original application *(see figure 2 item 13 in U.S. Patent 6,094,527)*. The Examiner asserts that the use of a hardware description language as disclosed in **Claims 9 and 38** of Applicant's current application where also supported in the parent application and are NOT new matter *(see Col. 3 Lines 7-13 of U.S. Patent 6,094,527 and independent Claim 2)*.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

**2.2** Regarding Applicants response to the Examiners rejection of Claims 1, 17, 25, 29, 33, 37 and 39 under obviousness-type double patenting;

Applicants have argued that;

> Claims 25, 29, and 37 were rejected under the judicially created doctrine of obviousness-type double patenting as allegedly unpatentable over claim 4 of U.S. Patent No. 6,094,527. Claims 33 and 39 were rejected under the judicially created doctrine of obviousness-type double patenting as purportedly unpatentable over claim 6 of U.S. Patent No. 6,094,527. Claim 1 was rejected under the judicially created doctrine of obviousness-type double patenting over claim 1 of U.S. Patent No. 6,094,527. Claim 17 was rejected under the judicially created doctrine of obviousness-type double patenting as allegedly unpatentable over claim 3 of U.S. Patent No. 6,094,527.
>
> Applicants maintain that the claims of the subject application are patentably distinct from the claims of U.S. Patent No. 6,094,527 for at least the following reasons.
>
> For example, claim 4 of U.S. Patent No. 6,094,527 recites an apparatus for estimating power consumption of an integrated circuit. Each of claims 25 and 29 of the subject application claims a programmable computer for estimating power consumption of an integrated circuit, and claim 37 claims a

programmed computer for estimating power consumption of an integrated circuit. Even if claims 25, 29, and 37 of the subject application can hypothetically be analogized to claim 4 of U.S. Patent No. 6,094,527, the comparison merely shows that claims 25, 29, and 37 of the subject application are species of a class of apparatuses for estimating power consumption of an integrated circuit. Applicants respectfully submit that species claims cannot be rendered unpatentable, even under the judicially created doctrine of obviousness-type double patenting, by patent claims to the broader class.

These same reasons apply similarly to the comparisons of claims 33 and 39 of the subject application and claim 6 of U.S. Patent No. 6,094,527.

In addition, each of claims 1 and 17 claims a computer readable medium including computer executable code stored thereon for estimating power consumption of an integrated circuit. The claimed invention can be regarded as species of a class of apparatuses for estimating power consumption of an integrated circuit. Each of claims 1 and 3 of U.S. Patent No. 6,094,527, in contrast, each recites a method for estimating power consumption of an integrated circuit. Applicants respectfully submit that method claims 1 and 3 of U.S. Patent No. 6,094,527 cannot render unpatentable claims 1 and 17 of the subject application, even under the judicially created doctrine of obviousness-type double patenting.

Accordingly, Applicants submit that independent claims 1, 17, 25, 29, 33, 37, and 39 are patentable over U.S. Patent No. 6,094,527.

The Examiner asserts that, as regards the non-statutory double patent rejections of Claims **25, 29 and 37** by **Claim 4 of U.S. Patent 6,094,527**, that a programmable computer is an *apparatus* and that a storage media for storing computer executable code, including code for carrying out logic simulations is a *simulation means* and that the programmable computer and the storage media for storing computer executable code are obvious ways in which a skilled artisan, at the time of the invention, would implement Applicant's claimed invention and therefore the Examiner upholds the earlier non-statutory rejection of **Claims 25, 29 and 37** by **Claim 4 of U.S. Patent 6,094,527.** The Examiner further asserts that a programmable computer and a storage media for storing computer executable code are well known in the art and the Examiner is not aware of any other method or apparatus combination that is available wherein Applicant's invention could be implemented in a practical manner. *Except for the use of a programmable computer with a storage means for executable code, how else could Applicant's*

*type of simulation be implemented?* As regards the non-statutory double patenting rejections of **Claims 33 and 39** by **Claim 6 of U.S. Patent 6,094,527** the Examiner asserts that the ONLY obvious *apparatus* for using Applicant's claimed invention is a programmable computer and the Examiner is unable to determine what other *apparatus,* at the time of the invention, could be used to implement Applicant's claimed invention. Examiner asserts that the only *simulation means* that is practical for implementing Applicant's claimed invention, at the time of the invention, is *storage means for executable code.* Applicant has opined that, "*Applicants respectfully submit that species claims cannot be rendered unpatentable, even under the judicially created doctrine of obviousness-type double patenting, by patent claims to the broader class*", Examiner asserts that Applicant has not presented any factual argument or cited any case law regarding species claims not being unpatentable under the judicially created doctrine of obviousness-type double patenting and therefore find Applicant's arguments to be unpersuasive. The Examiner asserts that, as regards the non-statutory double patent rejections of **Claim 1** by **Claim 1 of U.S. Patent 6,094,527** that the only *method* that would be obvious to one of ordinary skill in the art, at the time of Applicant's claimed invention to simulate and estimate the power consumption of an integrated circuit would be to store on a computer readable medium, executable code for estimating the power consumption of an integrated circuit. The Examiner asserts that, as regards the non-statutory double patent rejections of **Claim 17** by **Claim 3 of U.S. Patent 6,094,527** that the only *method* that would be obvious to one of ordinary skill in the art, at the time of Applicant's claimed invention to simulate and estimate the power consumption of an integrated circuit would be to store on a computer readable medium, executable code for estimating the power consumption of an integrated circuit. The Examiner has found Applicant's

arguments regarding the non-statutory double patenting rejections of **Claims 1, 17, 25, 29, 33, 37 and 39** to be unpersuasive and upholds the earlier non-statutory double patenting rejections.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

**2.3** Regarding Applicant's response to Examiners double patenting objection to Claims 29 and 25:

Applicant has argued that;

> Independent claim 29 was objected to under 37 C.F.R. §1.75 as allegedly being a substantial duplicate of independent claim 25. Applicants respectfully point out that MPEP §706.03(k) states that "court decisions have confirmed applicant's right to restate (i.e., by plural claiming) the invention in a reasonable number of ways. Indeed, a mere difference in scope between claims has been held to be enough. A comparison of claims 29 and 25 shows that claim 29 recites features not recited in claim 25. One non-limiting example of a feature recited in claim 29 that is not recited in claim 25 is that an estimate for a first value of electric power consumed by the basic cells is based on pre-established power consumption data for each logic state at each input and output terminal of the basic cells, among other factors.
>
> In addition, Applicants respectfully submit that such an objection is premature, since neither claim 25 or 29 have been allowed. Accordingly, Applicants respectfully request the objection under 37 C.F.R. §1.75 be withdrawn.

The Examiner has found Applicant's arguments to be persuasive in regards to the double patenting objection of Claims **29** and **25** and withdraws the earlier objection.

**2.4** Regarding Applicants response to Examiner Claim interpretation:

Applicant has argued that;

> The Office Action states that the broadest possible interpretation has been given to the claims, and interprets the "logic of basic and mega cells of an integrated circuit" as logic gates in an Application Specific Integrated Circuit (ASIC), and in the case of claims 9 and 38 a Field Programmable Gate Array (FPGA). According to the Office

Action, mega cells have been construed in the Office Action to mean the groups of transistors at the gate level of ASICs or FPGAs. Applicants respectfully disagree. The subject application explicitly incorporates by reference the entire contents of parent application no. 08/879,696 (see the present application, page 1 under "Cross-Reference to Related Applications"). Parent application no. 08/879,696 (at page 2, lines 17-18) states that basic cells are relatively simple logic gates including, for example, AND, OR, NOR, and NOT logic gates. According to parent application no. 08/879,696 (at page 2, lines 18-22), a mega cell may be defined by functional circuit blocks, functions of which are described by the hardware description language during logic simulations, and those cells whose construction is not explicitly represented by basic cells. Examples of mega cells include CPUs, DSPs, ROMs, and ROMs.

The Examiner asserts that Applicant has clarified the meaning of *"Mega cells"* and the Examiner finds Applicant's arguments to be persuasive in regards to the meaning of the phrase, *"Mega cells"*.

**2.5** Regarding Applicants response to the 35 U.S.C. 103(a) rejection of Claims 1-33:

Applicant has argued that;

Claims 1-39 were rejected under 35 U.S.C. §103(a) as allegedly unpatentable over U.S. Patent 5,943,487 to Messerman et al. in view of U.S. Patent No. 6,324,678 to Dangelo et al., and further in view of U.S. Patent No. 5,867,397 to Koza et al., and the Microsoft Press Computer Dictionary, Third Edition. Applicants have carefully considered the Examiner's comments and the cited art, and respectfully submit that independent laiins 1, 9, 17, 25, 29, 33, and 37-39 are patentable over the cited art, for at least the following reasons.

Independent claim 1 relates to a computer readable medium including computer executable code stored thereon, for estimating power consumption of an integrated circuit. The computer executable code includes (a) code for simulating logic of basic and mega cells of the integrated circuit, (b) code for estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and preestablished power consumption data, (c) code for estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and (d) code for combining the first and second values to obtain the power consumption of the integrated circuit.

Messerman et al., as understood by Applicants, relates to a method for reducing a full resistor network extracted from an integrated circuit polygon layout, and then simulating operation of the reduced resistor network to determine operational voltages at the nodes of the reduced resistor network. The operational voltages at the nodes of the full resistor network can then

be determined, as well as the operational current through a resistor utilizing the node voltages in the full resistor network (col. 3, lines 33-43, col. 9, lines 8-16, and col. 10, lines 30-38).
Dangelo et al., as understood by Applicants, relates to a method and system for creating and validating a low-level description of an electronic design. Static power dissipation is calculated by multiplying a leakage current (static current draw) of a representative logic device (gate) and a supply voltage, and summing the total number of logic devices (gates) (col. 36, line 66 to col. 37, line 17). Dynamic power dissipation in a CMOS device is calculated using output load capacitance, supply voltage, clock cycle, and the number of switching transitions per clock cycle as parameters (col. 37, lines 18-55). Power estimation at a system level uses statistical models that take into account critical parameters (col. 39, lines 18-67). Power estimation at algorithmic (functional), behavioral and register transfer levels utilizes more information. Control logic size and associated power dissipation are estimated from the number of states in the design and the complexity of Boolean equations activating elements of the data path in the circuit (col. 40, line 63 to col. 41, line 24).

However, Applicants find no teaching or suggestion in Dangelo et al. (or in the other cited references) of, for example, code for estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and preestablished power consumption data, as recited in independent claim 1.

Koza et al., as understood by Applicants, relates to a method and apparatus for automated design of complex structures such as circuits using genetic operations. The behavior of the developed structure is determined, compared to the predetermined design goals and then evolved until it meets the design goals (Fig. 1A, and col. 33-64). Simulations and fitness measures as discussed in Koza et al. focus solely on circuit behavior in terms of inputs and outputs (col. 80, line 46 to col. 83, line 35).
Applicants find no teaching or suggestion in the cited art of a computer readable medium including computer executable code stored thereon, the code for estimating power consumption of an integrated circuit, comprising code for simulating logic of basic and mega cells of the integrated circuit, code for estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component and a direct current component for each logic state to calculate the current consumed by the mega cells for estimating a first value of electric power consumed by the mega cells based on the logic simulations and preestablished power consumption data, code for estimating a current consumed by the basic cells for estimating a second value of electric power consumed by the basic cells based on the logic simulations and pre-established power consumption data, and code for combining the first and second values to obtain the power consumption of the integrated circuit, as recited in independent claim 1.

Accordingly, Applicants submit independent claim 1 is patentable over the cited art. Independent claims 9, 17, 25, 29, 33, and 37-39 are believed to be patentable over the cited art for at least similar reasons.

In addition, Applicants find no teaching or suggestion in the cited art of code for compiling a table which tabulates data of electric power consumed

by mega cells of the integrated circuit during operation, and code for simulating logic of the mega cells and basic cells of the integrated circuit, wherein data from the table is used when simulating logic of the mega cells, as recited in independent claims 17 and 39. Independent claim 33 is believed to be patentable for at least similar reasons.

The Examiner asserts that Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The Examiner has found Applicant's arguments to be a recitation of the claim language and upholds the earlier 35 U.S.C. 103(a) rejections of claims 1-33.

## ***Nonstatutory Double Patenting***

**3.** A rejection based on nonstatutory double patenting is based on a judicially created doctrine grounded in public policy so as to prevent the unjustified or improper timewise extension of the right to exclude granted by a patent. In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969); In re White, 405 F.2d 904, 160 USPQ 417 (CCPA 1969); In re Schneller, 397 F.2d 350, 158 USPQ 210 (CCPA 1968); In re Sarett, 327 F.2d 1005, 140 USPQ 474 (CCPA 1964).

**3.1 Claims 25-32 and 37** under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **Claim 4** of **U.S. Patent No. 6,094,527.** Although the conflicting claims are not identical, they are not patentably distinct from each other because the Claim in the Applicants application is describing an ***apparatus*** as in **Claim 4 of U.S. Patent 6,094,527.** One of ordinary skill in the art, at the time of the invention, would use a *programmable computer* as an apparatus for estimating power consumption because it would be faster than performing the calculations by hand. It would have been obvious, to have used a processor for executing computer executable code and to have had code for carrying out logic

simulations of circuit data for basic cells and mega cells as disclosed in **Claim 4** of **U.S. Patent 6,094,527.** The examiner notes that the only apparatus disclosed in **U.S. Patent 6,094,527** is a computer with computer readable media ***(see figure 2 in U.S. Patent 6,094,527).***

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

**3.2 Claims 33-36 and 39** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **Claim 6** of **U.S. Patent No. 6,094,527.** Although the conflicting claims are not identical, they are not patentably distinct from each other because the Claim in the Applicants application is describing an ***apparatus*** as in **Claim 6 of U.S. Patent 6,094,527.** One of ordinary skill in the art would use a *programmable computer* as an apparatus for estimating power consumption as regards a simulation, therefore it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have used a processor for executing computer executable code and to have had code for carrying out logic simulations of circuit data for basic cells and mega cells as disclosed in **Claim 6** of **U.S. Patent 6,094,527** because it would be faster than performing the calculations by hand. The examiner notes that the only apparatus disclosed in **U.S. Patent 6,094,527** is a computer with computer readable media ***(see figure 2 in U.S. Patent 6,094,527).***

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the

application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

**3.3** **Claims 1-8** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **Claim 1** of **U.S. Patent No. 6,094,527.** Although the conflicting claims are not identical, they are not patentably distinct from each other because the Claim in the Applicants application is describing a ***method*** steps encoded on media and **Claim 1** in U.S. Patent number 6,094,527 is claiming a method. For example, the Applicant is claiming in **Claim 1** of the Application that, *"a computer readable medium, including computer executable code stored thereon, the code..."* this portion is describing a method of performing applicant's simulation with the addition of a computer readable media, which was disclosed in applicant's first Patent as a hard disk *(see **figure 2 U.S. Patent 6,094,527 item 13**)* and is therefore is not patently distinct from **Claim 1** of **U.S. Patent No. 6,094,527**. Claim 1, of the patent, does not expressly recite "computer readable media". However it would have been obvious, by one of ordinary skill in the art, at the time of the invention, to have used computer readable media as this would have facilitated the use of the method on a computer.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

**3.4** **Claims 17-24** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **Claim 3** of **U.S. Patent No. 6,094,527**. Although the conflicting claims are not identical, they are not patentably distinct from each other

because the Claim in the Applicants application is describing the same invention as disclosed on **Claim 3** of **U.S. Patent number 6,094,527** is claiming a method. For example, the Applicant is claiming in **Claim 17** of the Application that, *"a computer readable medium, including computer executable code stored thereon, the code..."* this portion is describing a method of performing applicant's simulation with the addition of a computer readable media, which was disclosed in applicant's first Patent as a hard disk *(see **figure 2 U.S. Patent 6,094,527 item 13**)* and is therefore is not patently distinct from **Claim 3** of **U.S. Patent No. 6,094,527**. Claim 3, of the patent, does not expressly recite "computer readable media". However it would have been obvious, by one of ordinary skill in the art, at the time of the invention, to have used computer readable media as this would have facilitated the use of the method on a computer.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

**3.5** **Claims 9-16** are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **Claim 2** of **U.S. Patent No. 6,094,527**. Although the conflicting claims are not identical, they are not patentably distinct from each other because the Claim in the Applicants application is describing the same invention as disclosed on **Claim 2** of **U.S. Patent number 6,094,527** is claiming a method. For example, the Applicant is claiming in **Claim 9** of the Application that, *"A computer readable medium including computer executable code stored there, the code for estimating..."* this portion is describing a method of performing applicant's simulation with the addition of a computer readable media, which was

disclosed in applicant's first Patent as a hard disk *(see **figure 2 U.S. Patent 6,094,527 item 13**)* and is therefore is not patently distinct from **Claim 2** of **U.S. Patent No. 6,094,527**. Claim 2, of the patent, does not expressly recite "computer readable media". However it would have been obvious, by one of ordinary skill in the art, at the time of the invention, to have used computer readable media as this would have facilitated the use of the method on a computer.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

**3.6** **Claim 38** is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over **Claim 4** of **U.S. Patent No. 6,094,527**. Although the conflicting claims are not identical, they are not patentably distinct from each other because the Claim in the Applicants application is describing the same invention as disclosed on **Claim 4** of **U.S. Patent number 6,094,527** is claiming an apparatus. For example, the Applicant is claiming in **Claim 38** of the Application that, *"A programmed computer for estimating electrical power consumed by basic cells and mega cells of an integrated circuit..."* as an apparatus for estimating power consumption as regards a simulation, therefore it would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have used a processor for executing computer executable code and to have had code for carrying out logic simulations of circuit data for basic cells and mega cells as disclosed in **Claim 4** of **U.S. Patent 6,094,527** because it would be faster than performing the calculations by hand. The examiner notes that the only apparatus disclosed in **U.S. Patent 6,094,527** is a computer with computer readable media

***(see figure 2 in U.S. Patent 6,094,527).*** As regards the limitation concerning the use of a *hardware description language* this limitation was disclosed in applicant's original application and therefore the applicant had the opportunity to present the limitation of using a hardware description language in **U.S. Patent 6,094,527**, the Examiner further asserts that to properly use an programmable computer for the simulation as disclosed in applicant's application that it would have been obvious, to one of ordinary skill in the art, to have used a hardware description language.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968). See also MPEP § 804.

***Claim Rejections - 35 USC § 101***

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

**4.** **Claims 1-39** are rejected under 35 U.S.C. 101 because the claimed invention is not supported because the stored executable code, as it is disclosed in applicant's claim language, is never actually executed. The Applicant's claim language discloses that the computer readable media includes computer executable code the Claim language does not expressly disclose that the computer executable code is actually executed on the programmable computer and if it where to be executed the current claim language does not disclose exactly if both the code for simulating the logic of basic and mega cells is executed as well as the code for estimating the

current consumed by the mega cells is also executed and therefore there is no utility to applicant's invention.

**4.1** **Claims 1-39** are also rejected under 35 U.S.C. 112, first paragraph. Specifically, since the claimed invention is not supported because the stored executable code, as it is disclosed in applicant's claim language, is never actually executed. The Applicant's claims disclose that the computer readable medium includes executable code, there is no language in the claims that specifically describes the code actually being *executed* and therefore one skilled in the art clearly would not know how to use the claimed invention.

## ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**5.** **Claims 1-39** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Messerman et al. U.S. Patent 5,943,487** in view of **Dangelo et al U.S. Patent 6,324,678** and in further view of **Koza et al. U.S. Patent 5,867,397** and in further view "**Microsoft Press Computer Dictionary, Third Edition, *Published 1997*** here after referred to as the *Microsoft* reference.

**5.1** As regards **Claims 1, 25, 29 and 37** the *Messerman et al.* reference teaches the following limitations; A computer readable medium including executable code stored thereon, **(Figure 9 Items 410, 408 and 404),** code for simulating logic of an integrated circuit **(Figures 1-9 and Col. 1 Lines 46-58),** determining the direct current component for resistor network **(Col. 1**

**Lines 34-67 and Col. 2 Lines 1-8)**, code for estimating a current consumed by the resistor network for estimating a second value of electric power consumed by the resistor network and pre-established power consumption data and code for combining said first and second values to obtain the power consumption of the integrated circuit's resistor network **(Col. 1 Lines 12-67 and Col. 2 Lines 1-46 and Col. 7 Lines 44-63).**

The limitations not expressly disclosed in the *Messerman et al.* reference are, code for simulating logic of basic and mega cells of the integrated circuit, determining the average frequency of operation for each logic state, determining the alternating current component for each logic state consumed by the mega cell.

The *Dangelo et al.* reference teaches code for simulating logic of basic and mega cells of the integrated circuit, **(Figure 1 Item 116 and Figure 8 Items 824 as regards logic see Figure 12 Items 1214 and 1226, and mega-cells Col. 44 Lines 47-61)**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Dangelo et al.* reference because, *motivation to combine*, the *Dangelo et al.* reference discloses simulation of logic circuits as well as power estimation ***(Col. 36 Lines 35 –67and Col. 37 Lines 1-67 and Col. 38 Lines 1-9 and Col. 39 Lines 18-67 and Col. 40 Lines 1-67 and Col. 41 Lines 1-52).***

The *Koza et al.* reference discloses measuring the alternating current of each logic cell, **(Note VSOURCE in Figures 25-35 and VSOURCE in Figures 53-61 also note the Z terms in Figures 53-56, these relate to frequency dependent elements in the circuit, Note Figures 82-85, Note Figure 105, Note Figures 108 Item OR6 and Figure 107 Item AND6 and Col. 16 Lines 13-39).** *Examiners Note: As regards the Koza et al. reference to being analogous art*

*Examiner points out that this reference was issued in the 703/14 subclass entitled, "Simulating Electronic Device or Electrical System/Circuit simulation" a mega-cell in an ASIC or FPGA is an electronic device.*

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Koza et al.* reference because *(Motivation to combine)* by modeling the AC characteristics of each logic cell the designer is able to determine the fitness of each sub-circuit for its intended use ***(Koza et al. Col. 82 Lines 37-67 and Col. 83 lines 1-35).***

**5.2** As regards **Claims 9 and 38,** the *Messermann et al.* reference does not expressly disclose a Hardware Description Language.

The *Dangelo et al.* reference discloses a hardware description language as well as a computer system for simulating mega cells, **(Figure 8 item 604, all of Figure 9, all of Figure 10, 11, 12, 13, 18 and 19, and Col. 1 Lines 25-67 and all of Columns 3, 4. and Col. 5 Lines 1-36, Col. 8 Lines 38-67 and Col. 9-18 and Col. 19 Lines 1-57.)**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Dangelo et al.* reference because, *motivation to combine*, the *Dangelo et al.* reference discloses simulation of logic circuits as well as power estimation ***(Col. 36 Lines 35 –67and Col. 37 Lines 1-67 and Col. 38 Lines 1-9 and Col. 39 Lines 18-67 and Col. 40 Lines 1-67 and Col. 41 Lines 1-52).***

**5.3** As regards **Claims 17, 33 and 39,** the *Messermann et al.* reference does not expressly disclose compiling a table that tabulates data.

The *Dangelo et al.* reference discloses a compiling a table that tabulates data as well as a computer system for simulating mega cells, **(Figures 16a-b and Col. 5 Lines 56-63).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Dangelo et al.* reference because, *motivation to combine*, the *Dangelo et al.* reference discloses simulation of logic circuits as well as power estimation ***(Col. 36 Lines 35 –67and Col. 37 Lines 1-67 and Col. 38 Lines 1-9 and Col. 39 Lines 18-67 and Col. 40 Lines 1-67 and Col. 41 Lines 1-52).***

**5.4** As regards **Claims 2-8, and 10-16 and 18-24** the previous rejections disclosed above address all of the limitations for **Claims 1, 9 and 17.**

**5.5** As regards **Claim 2, 10 and 18,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a floppy disk.

The *Microsoft* reference discloses the use of a floppy disk **(Page 201).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the floppy disk is a known computer readable medium and by storing the program code on a computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

**5.6** As regards **Claim 3, 11 and 19,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a 3.5-inch floppy disk.

The *Microsoft* reference discloses the use of a 3.5-inch floppy disk **(Page 201).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the 3.5-inch floppy disk is a known computer readable medium and by storing the program code on a computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

**5.7** As regards **Claim 4, 12 and 20,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a compact disk.

The *Microsoft* reference discloses the use of a compact disk **(Page 82).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the compact disk is a known computer readable medium and by storing the program code on a computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

**5.8** As regards **Claim 5, 13 and 21,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a read-only compact disk.

The *Microsoft* reference discloses the use of a read-only compact disk **(Page 82).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the

compact disk is a known computer readable medium and by storing the program code on a computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

**5.9** As regards **Claim 6, 14 and 22,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a read/write compact disk.

The *Microsoft* reference discloses the use of a read/write compact disk **CD-R (Pages 81, 82).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the compact disk is a known computer readable medium and by storing the program code on a computer readable medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

**5.10** As regards **Claim 7, 15 and 23,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of a DVD.

The *Microsoft* reference discloses the use of a **DVD (Pages 145-146).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because the DVD is a known computer readable medium and by storing the program code on a computer readable

medium the user does not have to manually program the computer every time the computer executable code needs to be executed.

**5.11** As regards **Claim 8, 16 and 24,** the *Messerman et al.* reference discloses the use of a computer readable medium for executing code **(Figure 9, Items 408 and 404).**

The *Messerman et al.* reference does not expressly disclose the use of computer executable code that is compressed and non-compressed.

The *Microsoft* reference discloses the use of computer executable code **(Pages 182-183)** and compressed data **(Page 107)**.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because by compressing the computer executable code less storage space is required on the computer readable medium.

**5.12** As regards **Claims 26, 30 and 34,** the *Messerman et al.* reference discloses a programmable computer in comprising a read/write unit in which a computer readable media including computer executable code can be input, the computer executable code being downloaded from the computer readable media via the read/write unit for execution by the processor **(Figure 9)**.

**5.13** As regards **Claims 27, 31 and 35**, a programmable computer wherein the computer executable code is stored on computer readable media is discloses in **(Figure 9)** of the *Messerman et al.* reference.

However the *Messerman et al.* reference does not expressly disclose the executable code on the computer readable medium being in compressed format and is decompressed and downloaded to the storage media.

The *Microsoft* reference discloses executable code **(Page 182,183)** and a compressed format **(Page 107)**.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because, by compressing the executable code, storage space is conserved on the computer readable medium.

**5.14** As regards **Claims 28, 32 and 36** the *Messerman et al.* reference discloses a programmable computer with a computer readable medium **(Figure 9).**

The *Messerman et al.* reference does not disclose at least one of a floppy disk, a CD, DVD and an Internet server.

The *Microsoft* reference discloses, a floppy disk **(Page 201)** a CD *or Compact Disk* **(Pages 81-82)** a DVD **(Pages 145 and 146)** and an Internet server **(Page 430).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to have modified the *Messerman et al.* reference with the *Microsoft* reference because by storing the computer executable code on various computer readable medium the computer user does not need to re-enter the program code each time the code needs to be run and by using an internet server the program code can be accessed by any computer connected to the internet.

*Note to the Applicant, the examiner has disclosed examples in each of the references that disclose the elements in applicant's claim for invention, the examiner directs the attention of*

*Applicant to the Abstract, Backround of the Invention, Preferred embodiment, and Claims of the references sited.*

**6.** **Claims 1- 39** are rejected under 35 U.S.C. 103(a) as being unpatentable in view of **Raman et al. U.S. Patent 5,535,370** in view of **Crafts et al. U.S. Patent 5,521,834** and in further view of **Dangelo et al. U.S. Patent 5,493,508.**

**6.1** As regards **Claims 1, 9, 17, 25, 29, 33, 37, 38 and 39** the *Raman et al.* reference discloses a method of calculation of power using a circuit simulation **(Figures 1-3),** using a lookup table with pre-established power consumption data **(Figure 1 Item 50, Col. 4 Lines 59-65),** for each logic state **(Figures 4(a), 4(b)),** determining the average operation frequency **(Figure 1 Item 20, Col. 1 Lines 50-64),** determining a direct current for each node **(Figure 3 Item 220, Figures 4(c) and 4(d), 6b, 7, Col. 1 Lines 65-67, Col. 2 Lines 1-31),** basic cells **(Col. 4 Lines 66-67, Col. 5 Lines 1-52),** and portions of a mega cell **(Col. 6 Lines 56-67, Col. 7 Lines 1-4).**

The *Ramen et al.* reference does not expressly disclose calculating the alternating current component for each cell.

The *Crafts et al.* reference discloses calculating the alternating current component for each cell **(Figure 2 Items 30, 32, 34, Col. 4 Lines 1-67, Col. 5 Lines 1-10).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Ramen et al.* reference with the *Crafts et al.* reference because, *(motivation to combine)* the *Crafts et al.* reference discloses a better approach that is more accurate to calculate the power dissipated in a CMOS IC *(Crafts et al. Col. 6 Lines 31-62).*

The *Ramen et al.* reference does not expressly disclose mega-cells and hardware description languages.

The *Dangelo et al.* reference discloses mega-cells **(Col. 11 Lines 1-4),** and hardware description languages **(Col. 11 Lines 49-55).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention to have modified the *Ramen et al.* reference with the *Dangelo et al.* reference because, *(motivation to combine)* the *Dangelo et al.* reference discloses an improved method of simulating mega-cells with a hardware description language *(Dangelo et al. Col. 4 Lines 13-67).*

**6.2** As regards independent **Claims 25, 29, 30, 33, 34, 37, 38 and 39** the *Ramen et al.* reference does not expressly disclose a programmable computer.

The *Craft et al.* reference discloses a programmable computer **(Figure 1).**

It would have been obvious, to one of ordinary skill in the art, at the time of the invention, to have modified the *Ramen et al.* reference with the *Crafts et al.* reference because, *(motivation to combine)* the *Crafts et al.* reference discloses a better approach that is more accurate to calculate the power dissipated in a CMOS IC *(Crafts et al. Col. 6 Lines 31-62).*

**6.3** As regards independent **Claims 1, 9 and 17** the *Ramen et al.* reference does not expressly disclose a computer readable medium with computer executable code.

The *Dangelo et al.* reference discloses a computer readable medium with computer executable code **(Col. 8 Lines 47-67).**

It would have been obvious to one of ordinary skill in the art, at the time of the invention to have modified the *Ramen et al.* reference with the *Dangelo et al.* reference because,

*(motivation to combine)* the *Dangelo et al.* reference discloses an improved method of simulating mega-cells with a hardware description language *(Dangelo et al. Col. 4 Lines 13-67)*.

## ***Conclusion***

7. **Claims 1-39** are rejected under 35 U.S.C. 103(a), 35 U.S.C. 101 and Non-statutory Double Patenting. An updated search has revealed new art.

**7.1** In view of Examiners new rejections of **Claims 1- 39** under 35 U.S.C. 103(a) and 35 U.S.C. 101 and the Non-statutory Double Patenting of **Claims 1- 39** this action is made **NON-FINAL.**

**7.2** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M Craig whose telephone number is 703 305-7150. The examiner can normally be reached on 10:00 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

DMC
May 27, 2003

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
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